REMARKS

Claims 1-61 are pending, with claims 1, 12, 23, 36, 50, 54, and 58 being independent. Claims 54-61 are withdrawn. Claim 50 is amended by virtue of this amendment, and claim 1 is amended to correct an informality.

Claims 23-49 are allowed. Applicant thanks the Examiner for allowing these claims.

Claims 1-11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of co-pending U.S. Application No. 09/931,061 (the '061 application). Claims 12-22 also are provisionally rejected under the judicially created doctrine of obviousness-type double patenting, as being unpatentable over claims 11-20 of the '061 application. Claims 23-35 also are provisionally rejected under the judicially created doctrine of obviousness-type double patenting, as being unpatentable over claims 21-32 of the '061 application. Finally, claims 36-49 also are provisionally rejected under the judicially created doctrine of obviousness-type double patenting, as being unpatentable over claims 33-45 of the '061 application. Applicant requests that these provisional double-patenting rejections be held in abeyance and re-evaluated upon allowance and issue of the '061 application.

Claims 1, 4, 9-12, 15, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,246,386 to Perner (Perner) in view of U.S. Patent No. 4,432,610 to Kobayashi (Kobayashi). Claims 2, 3, 5, 13, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner in view of Kobayashi, and further in view of U.S. Patent No. 5,699,078 to Yamazaki et al. (Yamazaki). Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner in view of Kobayashi, and further in view of U.S. Patent No. 5,471,225 to Parks (Parks). Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner in view of Kobayashi and Parks, and further in view of U.S. Patent No. 5,945,866 to Fonash et al. (Fonash). Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner in view of Kobayashi and Parks, and further in view of U.S. Patent No. 4,752,118 to Johnson et al. (Johnson).

Claims 50-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Perner.

Regarding preliminary matters, Applicant thanks the Examiner for acknowledging Applicant's claims to priority under 35 U.S.C. 119, and for returning initialed versions of the previously-submitted Forms PTO-1449. Applicant requests that the Examiner acknowledge acceptance of the drawings filed with the present application.

Regarding the rejection of claims 1, 4, 9-12, 15 and 20-22 under 35 U.S.C. 103(a) as being unpatentable over Perner in view of Kobayashi, Applicant respectfully submits that proper motivation to combine these references in the proposed manner has not been established, so that the proposed combination of Perner and Kobayashi does not validly support a prima facie case of obviousness under 35 U.S.C. 103(a).

For example, independent claim 1 recites, "A liquid crystal display device having a plurality of pixels, **each of the plurality of pixels comprising a plurality of memory circuits and a plurality of non-volatile memory circuits**." The rejection maintains that Perner discloses a liquid crystal display device having a plurality of pixels comprising a plurality of memory circuits, but acknowledges that Perner does not disclose such pixels comprising "a plurality of non-volatile memory circuits," as recited in claim 1.

Rather, the rejection maintains that Kobayashi provides such a teaching, and that incorporation of the non-volatile memory circuits of Kobayashi in the LCD device pixels of Perner would have been obvious for "maintaining a last picture being displayed before the device is either shutdown ... or unplugged ..." (Office Action, paragraph 6).

In response, Applicant respectfully submits that Perner merely teaches the use of a plurality of memory circuits, and Kobayashi merely teaches the use of a plurality of non-volatile memory circuits. Neither reference teaches or properly suggests the combination of a plurality of memory circuits and a plurality of non-volatile memory circuits in each of a plurality of LCD device pixels, as recited in independent claim 1.

In particular, even if Kobayashi is read to provide a teaching of using non-volatile memory circuits to maintain "a last picture being displayed," this teaching alone does not

provide proper motivation or suggestion to use such circuits in combination with memory circuits in the same pixel(s). That is, Kobayashi, at best, merely discloses an advantage of non-volatile memory circuits, but the concept of including such non-volatile memory circuits in a pixel(s) with other memory circuits is found only in Applicant's specification.

Further, Applicant notes that a prima facie case of obviousness requires, in part, "a reasonable expectation of success" for a proposed combination (see MPEP 2143.02). In this case, operation of an LCD device and associated pixels and circuits clearly requires various circuit design issues, including, for example, how to fabricate the pixels, how to provide power to the circuits, and how to provide a workable timing for operating the pixels to provide a display (e.g., timing for display periods, memory writing periods, and so on).

The present rejection does not address any of these or related issues that would arise in creating a "plurality of pixels comprising a plurality of memory circuits and a plurality of non-volatile memory circuits." Nor does the rejection establish that such modifications would have been within the skill of one of ordinary skill in the art.

In short, the rejection merely points to two references that each arguably contain individual elements recited in claim 1, and states that some of these elements (circuits) provide an advantageous feature. However, there are many circuits that contain advantageous features, and this fact alone does not suggest that all such circuits could have been, or would have been, combined. As a result, Applicant respectfully submits that the reasoning of the rejection is incomplete at best, and that the rejection therefore does not support a valid prima facie case of obviousness under 35 U.S.C. 103(a).

Independent claim 12 also recites at least the inclusion of memory circuits and non-volatile memory circuits within a pixel of an LCD device, and therefore should be allowable over the pending 103(a) rejection for at least the same reasons set forth above. As a result, Applicant respectfully submits that dependent claims 2-11 and 13-22 are allowable over the pending 103(a) rejection for at least the same reasons.

Regarding the rejection of claims 50-53 under 35 U.S.C. 103(a) as being unpatentable over AAPAin view of Perner, Applicant respectfully submits that neither AAPA nor Perner,

whether taken alone or in combination, teaches all of the features of independent claim 50, as amended. In particular, the rejection maintains that Perner teaches the feature of original Claim 50 that, "one of the following (a) through (e) is conducted in pixels in the row of the selected gate signal line out of the plural pixels," which is (admittedly) not taught in AAPA.

However, Applicant respectfully submits that Perner does not disclose or properly suggest the feature of amended Claim 50 that "the following (a) through (e) are available and one of the following (a) through (e) is selected and conducted in pixels in the row of the selected gate signal line out of the plural pixels" (nor is such a feature disclosed or properly suggested in AAPA). For example, Perner does not teach the recited element of "(d) the n bit digital video signals stored in the non-volatile memory circuits are read" is selected and conducted in pixels.

Accordingly, Applicant respectfully submits that claim 50 is in condition for allowance, so that dependent claims 51-53 also are in condition for allowance for at least the same reasons. As already stated, claims 1-22 are believed to be in condition for allowance (pending resolution of the provisional double-patenting rejections set forth above), and claims 23-49 are allowed.

Based on the above, all claims are believed to be in condition for allowance (again, pending resolution of the provisional double-patenting rejections set forth above).

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Respectfully submitted,

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William G. Hughes, Jr.
Reg. No. 46,112

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331
WXH/adt
40200651.doc